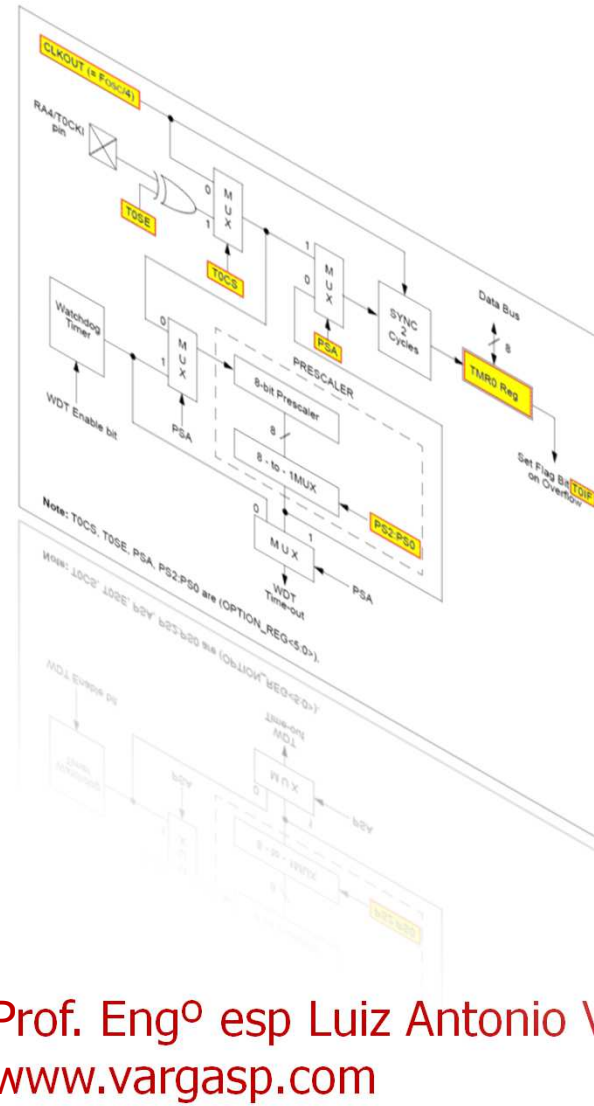
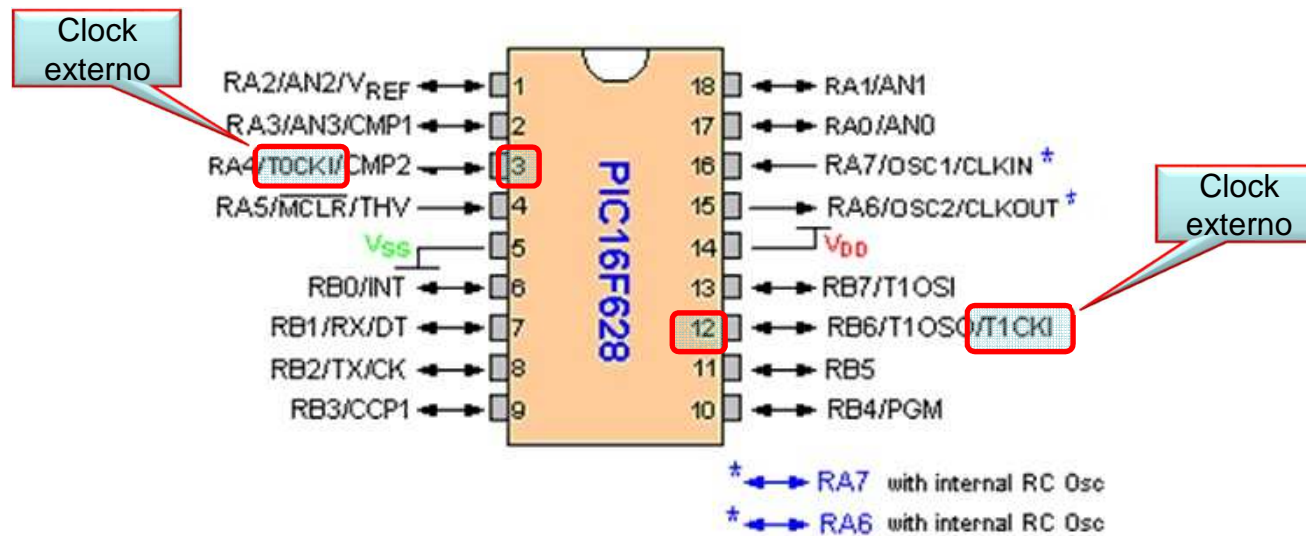


TIMER 0

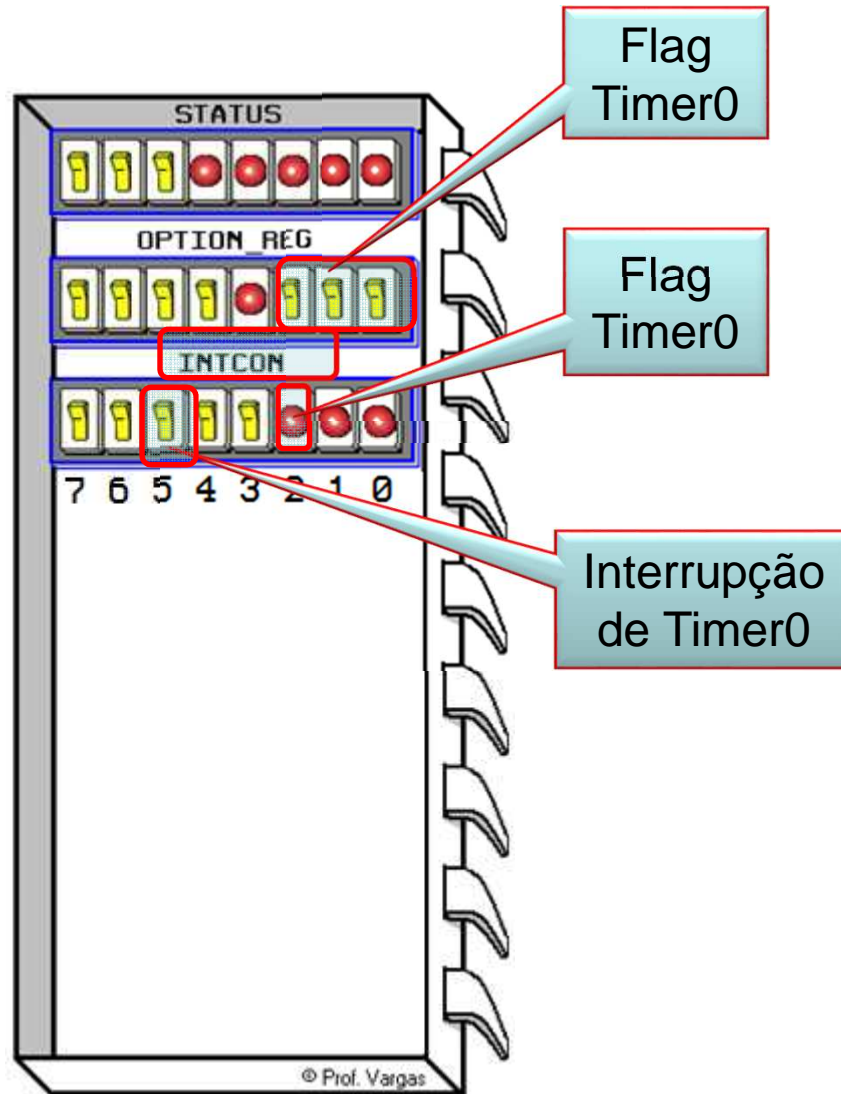


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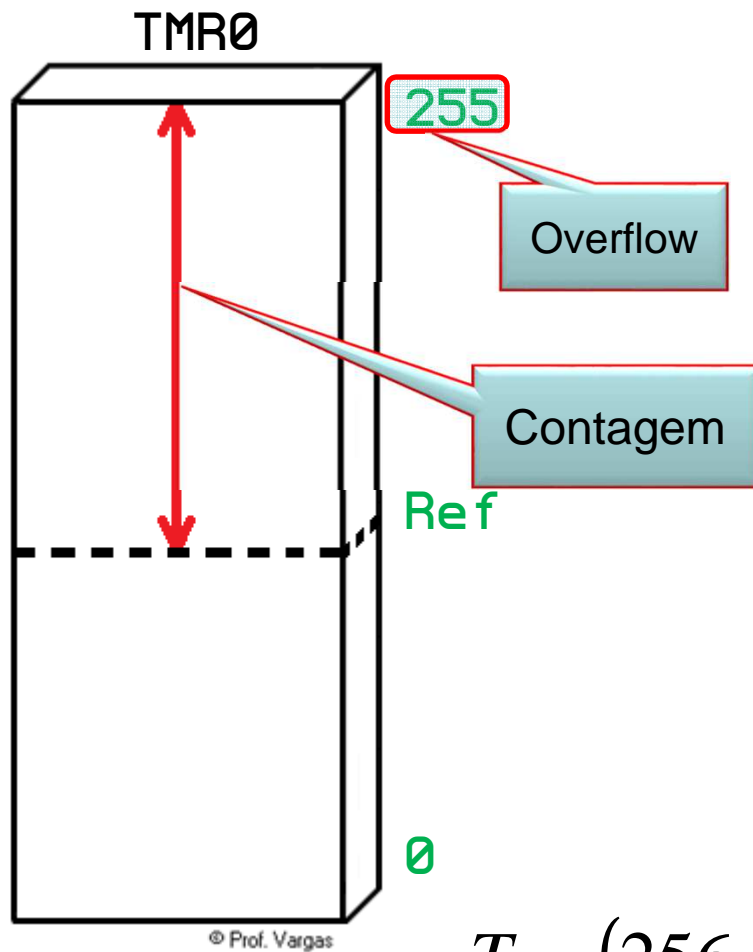
Características



Visão geral



O conceito



Bank 0		Bank 1		Bank 2		Bank 3	
Indirect addr. ⁽¹⁾	File Address	Indirect addr. ⁽¹⁾	File Address	Indirect addr. ⁽¹⁾	File Address	Indirect addr. ⁽¹⁾	File Address
TMR0	00h	OPTION	80h	TMR0	100h	OPTION	180h
PCL	01h	PCL	81h	TMR0	101h	OPTION	181h
STATUS	02h	PCL	82h	PCL	102h	PCL	182h
FSR	03h	STATUS	83h	STATUS	103h	STATUS	183h
PORTA	04h	FSR	84h	FSR	104h	FSR	184h
PORTB	05h	TRISA	85h		105h		185h
	06h	TRISE	86h	PORTE	106h	TRISE	186h
	07h		87h		107h		187h
	08h		88h		108h		188h
	09h		89h		109h		189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch		10Ch		18Ch
	0Dh		8Dh		10Dh		18Dh
TMR1L	0Eh	PCON	8Eh		10Eh		18Eh
TMR1H	0Fh		8Fh		10Fh		18Fh
T1CON	10h		90h				
TMR2	11h		91h				
T2CON	12h	PR2	92h				
	13h		93h				
	14h		94h				
CCPR1L	15h		95h				
CCPR1H	16h		96h				
CCP1CON	17h		97h				
RCSTA	18h	TXSTA	98h				
TXREG	19h	SPBRG	99h				
RCREG	1Ah	EEDATA	9Ah				
	1Bh	EEADR	9Bh				
	1Ch	EECON1	9Ch				
	1Dh	EECON2 ⁽¹⁾	9Dh				
	1Eh		9Eh				
CMCON	1Fh	VRCON	9Fh				
	20h		A0h	General Purpose Register 80 Bytes	11Fh-120h		
General Purpose Register 80 Bytes	20h-6Fh	General Purpose Register 80 Bytes	A0h-EFh				
	6Fh-70h	accesses 70h-7Fh	EFh-F0h				
16 Bytes	70h-7Fh		FFh	accesses 70h-7Fh	11Fh-120h		

□ Unimplemented data memory locations, read as '0'.
Note 1: Not a physical register.

$$T = (256 - TMR0) \times \frac{4}{F_{osc}} \times \text{Prescaler}$$

Prescaler (Registro Option_reg)

- Bit 3: **PSA**: Configuração do prescaler:

- 0 - prescaler aplicado ao TMR0.
- 1 - prescaler aplicado ao WDT.

- Bit 2,1,0: **PS2,PS1,PS0** :Configuração de prescaler:

PS2/1/0	TMR0	WDT
000	1:2	1:1
001	1:4	1:2
010	1:8	1:4
011	1:16	1:8
100	1:32	1:16
101	1:64	1:32
110	1:128	1:64
111	1:256	1:128